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# Signal Integrity Analysis and Compliance Test of PCIe Gen3 Serial Channel with IBIS-AMI

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White Paper from  
DesignCon 2017

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# DesignCon 2017

## Signal Integrity Analysis and Compliance Test of PCIe Gen3 Serial Channel with IBIS-AMI

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## **Abstract**

In this paper, signal integrity analysis and Compliance testing of complete PCIe Gen3 channel with IBIS-AMI model is presented. Gigahertz serialization and deserialization (SERDES) has become a leading inter-chip and inter-board data transmission technique in high-end computing devices. The IBIS-AMI model is used for circuit simulation of high-speed serial interfaces. The simulations are performed to ensure that the interface specifications are met, including the eye characteristics, and that the bit error rate (BER) is less than a specified maximum. A 3D frequency-domain simulator (FEM) was used to estimate the channel loss for data bus and PCIe connector. Compliance testing is performed for x8 PCIe channels to ensure channel parameters are meeting PCIe SIG specifications.

## **Authors Biography**

**Anil Pandey** is currently a master level Technical Leader in Keysight Technologies EEsof RnD section. He has more than 14 years' experience in RF, Microwave, Signal Integrity and Power Integrity analysis for high speed systems and Antenna Design. His areas of interest are Signal Integrity, Power Integrity, EMI/EMC, RF/Microwave circuits and Antenna designs. Anil Pandey has served as a reviewer for many international journals, such as IET, ACES and Antenna Journal and has been. He has delivered invited talks in various conferences and institutions including IIT Jodhpur, SSPL Delhi etc. He has more than 29 international and nation research publications and 2 patents to his credit. Apart from academics, his hobbies are creative writing and reading books.

## **I. Introduction**

With increased data rates of high-speed input/output I/O buses, maintaining the signal quality of the transmission channel becomes challenging due to parasitic effects from interconnects which did not impact the overall performance at lower data rates. Over the past decade, data rates for electrical interconnects have experienced a dramatic increase from 1 GB/s to 25 GB/s and beyond to meet ever increasing demands of more I/O bandwidth from modern networking applications and high-capacity storage.

SERDES is a high-speed serial data link used in integrated circuits (ICs) to serialize the parallel data and transfer it at a much faster rate. A typical SERDES architecture looks like a communication set-up with a transmit and a receive side. At transmit side, a PLL generates the fast clock necessary to drive the serializer. A clock and data recovery (CDR) circuit recovers a clock from the transmitted serial data and retimes the data at the receive side. One advantage of using SERDES is reduced clock skew, so data can be sent at the GHz rate. The main disadvantage in SERDES is timing jitter, the deviation of the actual signal transition from the expected transition in time. Timing skew is not a problem in serial interface because in each data lane, there is only one differential signal in each direction, and there is no external clock signal since clocking information is embedded within the serial signal itself.

PCI Express (PCIe) is one example of serial interconnects. The development of PC Express was driven by the need for much greater performance. PCI Express using high speed, 8Gbit/s serial links can suffer from a large array of physical phenomena including crosstalk, impedance discontinuities resulting in reflections (causing jitter), intersymbol interference, and mode conversion due to unbalanced transmission lines can lead to excessive EMI emissions in a large system. Signal Integrity Analysis and compliance testing is carried out to ensure high signal quality.

## **II. PCI Express Gen3 (PCIe 3.0) Interface**

PCI Express is the next generation Peripheral Component Interconnect (PCI) standard. The third generation, PCI Express Gen3, is a high speed differential I/O interconnects that runs at 8.0 Gigabits/second, it is widely used in computers and servers. Fig. 1 shows a typical PCIe Gen3 link, the channel could be short and straightforward with only a few inches of interconnect between the driver and the receiver, or could be long and complicated. The PCIe 3.0 channel can consist of anywhere from one to 32 lanes. The PCIe standard defines connectors for multiple widths: x1, x4, x8, x12, x16 and x32, where x represents lane.

A lane has two differential signaling pairs, with one pair for transmitting data and the other for receiving. Thus, each lane is composed of four signal traces. Each lane is used as a full-duplex byte stream, sending data packets in eight-bit format simultaneously in both directions between TX and RX of a link. PCI Express Gen3 uses 128b/130b encoding scheme as compare to 8b/10b encoding scheme in previous generations. This

encoding scheme reduces the bandwidth overhead from 20% of PCIe Gen2 to approximately 1.54% by using a technique called "scrambling".

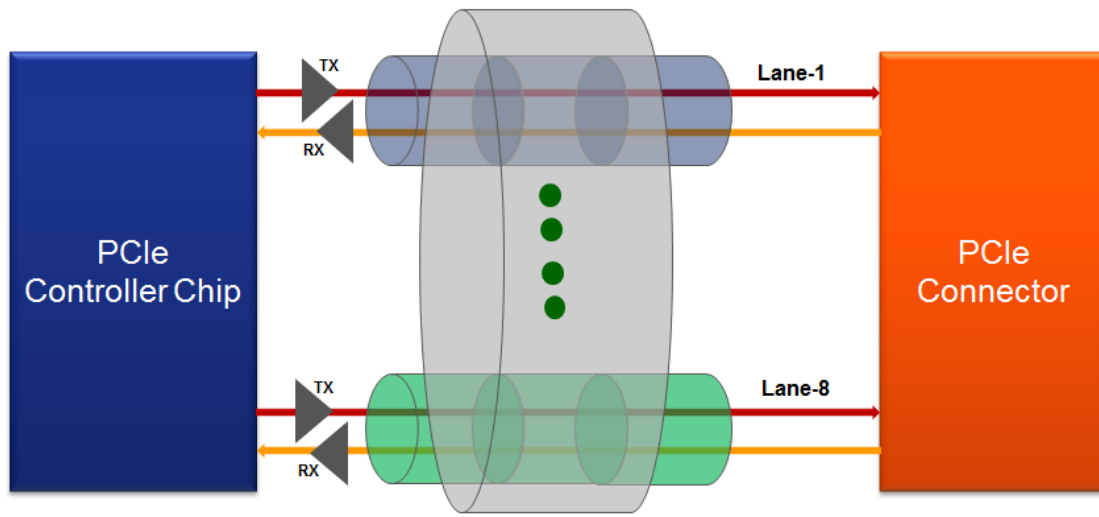


Figure 1: A typical 8-lane PCIe Gen3 link

### III. PCI Interface Simulation Methodology

As serial channels moved to high data rates, the IBIS AMI based signal integrity simulation method is used to account different channel parameters. In general, a time domain transient simulation utilizing IBIS AMI 5.0 transmitter and receiver models combined with lossy channel parameters are used to produce eye diagrams at a receiver end. Results are compared with received Eye Mask as per PCIe 3.0 requirement; if the simulated eye is within the eye opening specification for amplitude and jitter, then a better-than-specified BER (usually 12-17) would be achieved.

Performing a circuit simulation on a high-speed serial interface requires circuit models of the transmitter (TX) and receiver (RX), transmission line models of the die, package, PCB traces, vias and connectors that interconnect the elements. A time domain based circuit simulator combines these model elements, supplies a pseudo-random bit sequence (PRBS) stimulus to excite the current and voltage waveforms and Eye probes to observe the response. The passive components of the link are collectively called the channel. To ensure high quality signal, it is important to carefully design all aspects of these passive channel interconnects. A good practice is to create a virtual prototype of the entire link in a signal integrity EDA (electronic design automation) tool and simulate the eye diagram performance. The main objective of Signal Integrity analysis and compliance test is to optimize channel performance as per PCIe SIG specifications. The workflow of signal integrity analysis channel is shown in fig. 2. First, PCIe 3D connector is simulated using Finite Element Method (FEM) and S-parameter data is extracted then PCIe lanes are analyzed using full 3D EM simulator to get EM data. Both connector and PCIe data

bus simulation data is combine in transient analysis for complete link analysis with IBIS-AMI Models.

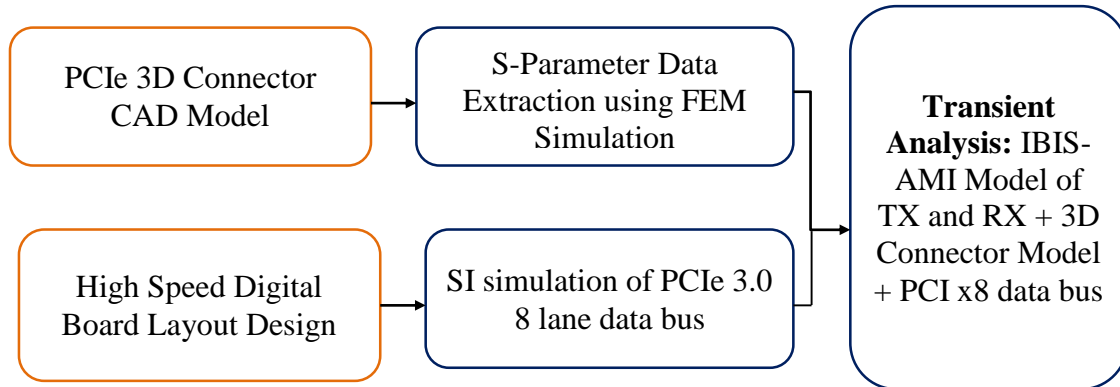


Figure 2: PCIe Gen3 Signal Integrity Analysis workflow

## 1. IBIS-AMI Model in simulation

The IBIS (Input/output Buffer Information Specification) models are a behavioral model using I-V and V-t look-up tables that make simulations extremely fast. At 8 Gb/s with interconnect of significant length and with the decision-feedback equalizer (DFE) and feed-forward equalizer (FFE), the IBIS specification is no longer sufficient to represent the TX and RX circuits and to overcome this problem an extension to IBIS has been developed known as IBIS-AMI (Algorithmic Modeling Interface). The IBIS-AMI model enables fast, accurate, statistically significant simulation of multi-gigabit serial links.

## 2. Jitters

It is known that the clock is embedded along with the transmitted data in serial communication systems and the clock data recovery (CDR) circuit is used to recover the clock at the receiver side. Latching the correct data depends strongly on the alignment between data and clock; jitter plays an important role in number of bit errors. Jitter can be classified into random jitter (RJ) and deterministic jitter (DJ). These jitter elements need to be included in simulation to simulate an accurate estimate of the BER.

## 3. Channel Simulation

The analysis approach outlined in this paper involves transient simulation whose length is determined by the amount of channel loss and the strength of reflections. The longer the channel, the more the inter symbol interference degrades the eye and the larger the number of random simulated bits required to approximate the worst-case pattern seen in actual system operation. The PCIe simulations were run at 8Gbps (UI=125ps). Simulations were run with IBIS-AMI models at TX and RX, including jitter at TX and with a channel length of 6 inches. The 8-lane PCI Express edge connector performs data transfers at the rate of 8.0 GT/s. The PCIe transmit and receive signal data paths have a

characteristic impedance of  $100\Omega \pm 10\%$ . The PCIe clock is routed as a  $100\Omega$  differential pair.

## 4. Equalization

PCIe 3.0 specification has the provision of performing Equalization at the transmitter and/or at the receiver to mitigate the effect of ISI and hence, to minimize the bit error rate (BER). In Equalization, the signal is passed through a Filter having its frequency response equal to inverse of frequency response of the channel. A high gain is applied at higher frequency to counter the signal attenuation at the high frequencies. In simple words, Equalization is an adaptive filter with coefficients determined on runtime depending upon the physical channel as shown in fig. 3.

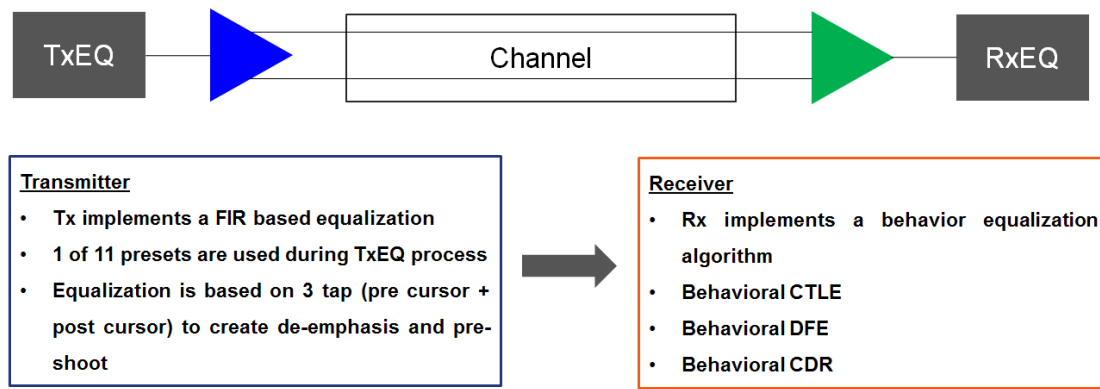


Figure 3: PCIe 3.0 Equalization at Transmitter and Receiver

## 5. De-emphasis and Pre-shoot

PCI Express uses transmit de-emphasis to compensate for high frequency channel losses. A de-emphasized waveform is defined in terms of the voltage levels called Vshelf (Va) and Vswing (Vb). Vshelf is calculated first for a given level of de-emphasis, using the equation 1 and 2. The resultant output signal when a binary input stream is applied to a 3-tap FIR Filter is shown in fig. 4. It can be seen that the output takes a different value just before and after polarity inversion of the input bit stream. Corresponding to these events, PCIe 3.0 specification defines new terminologies as explained in table 1. Voltages Va, Vb, Vc, and Vd correspond to De-emphasis, Flat Level, Pre-shoot and Maximum boost events, respectively.

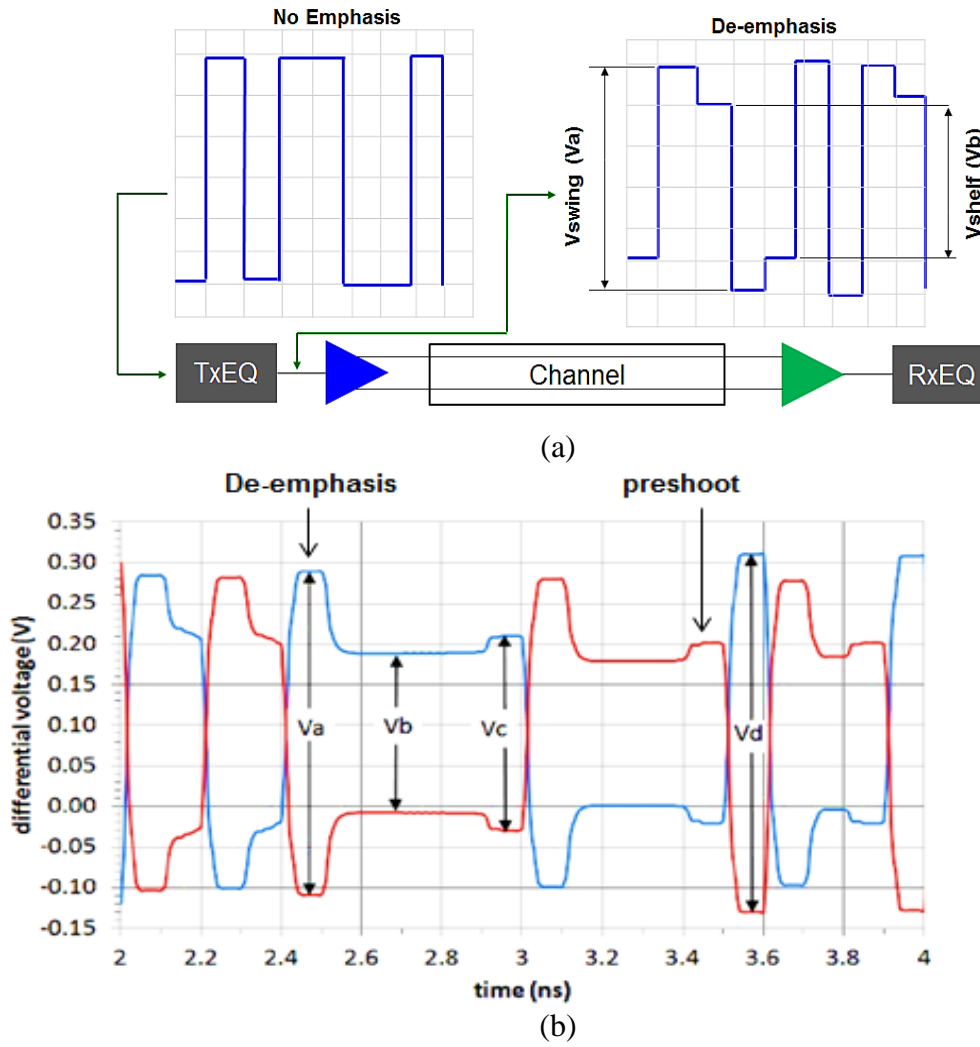


Figure 4: De-emphasis and Preshoot

PCIe 3.0 Term	Corresponding Condition on Input signal
De-emphasis (Va)	A boost appears just after the polarity inversion
Maximum Boost (Vb)	A major boost appears when there is polarity inversion only for one-bit interval
Pre-Shoot (Vc)	A boost appears just before the polarity inversion
Flat Level (Vd)	A constant voltage will appear when bits of the same polarity are being transmitted

Table 1: Different Equalization Terminologies

$$dB_{emphasis} = 20 * \log\left(\frac{V_b}{V_a}\right) \dots\dots\dots(1)$$

$$dB_{preshoot} = 20 * \log\left(\frac{V_c}{V_b}\right) \dots\dots\dots(2)$$

## IV. PCIe Simulations and Result

In the first phase of the design process, PCIe connector, eight lane data bus and package is simulation and EM data is extracted. In second phase all these data re combined and a pseudo-random bit sequence (PRBS) is generated at a bit rate of 8 Gbps.

### 1. PCIe 3.0 Connector Simulation and Result

High-speed connector is designed and simulated using Finite Element method (FEM). From this analysis, important factors from a Signal Integrity point of view (e.g., impedance matching, reflection, attenuation, impedance mismatch, propagating delay, crosstalk, and alignment shapes of connectors) are analyzed. In order to minimize impedance effects, the connector contact geometry is designed to keep the impedance profile as flat as possible. Fig 5(a) displays the 3D model and pin configuration of the PCIe connector. 32 pins are used as 16 pair of differential signals for 8 lanes. Simulated return loss is shown in fig. 5(b). The return loss is better than -9 dB while the insertion loss is less than -1.5 dB over the band (0-8 GHz).

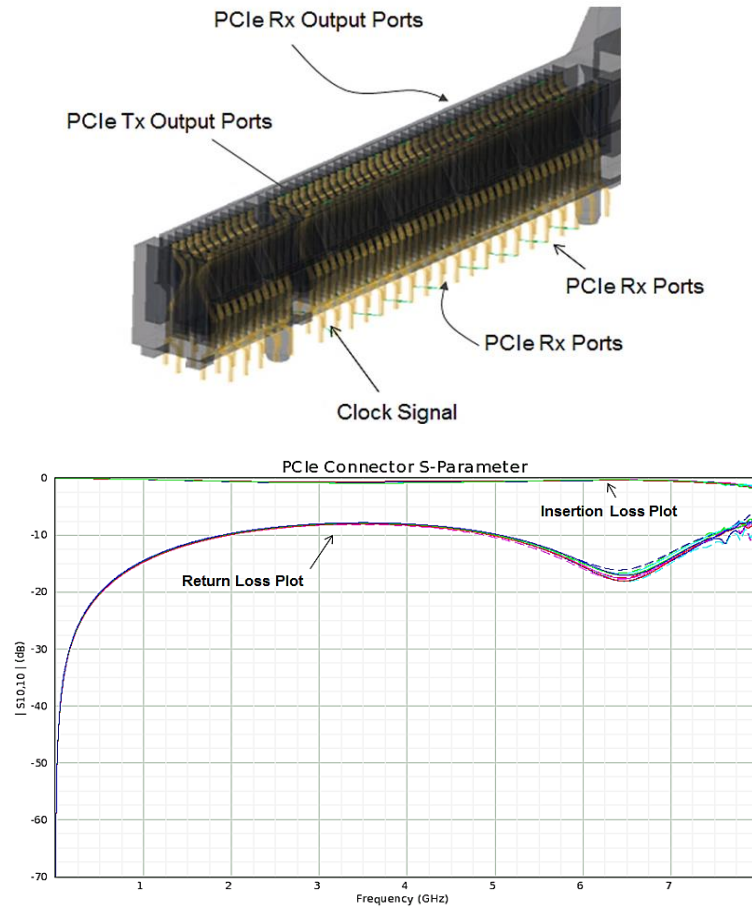


Figure 5: (a) PCIe 3.0 Connector (b) Simulation Result

## 2. 8 lane Data Bus Simulation

HSD board presented in this paper is a 12-layer high-speed FPGA digital board. The noise in channel network mainly affects the system jitter performance. This causes degradation in signal quality. For horizontal & vertical transitions, like wire bonds, via array, and solder balls of package and PCB, 3D models were generated for SI/PI simulations. EM simulated data is extracted for PCIe 3.0 eight-lane data bus shown in fig. 6.

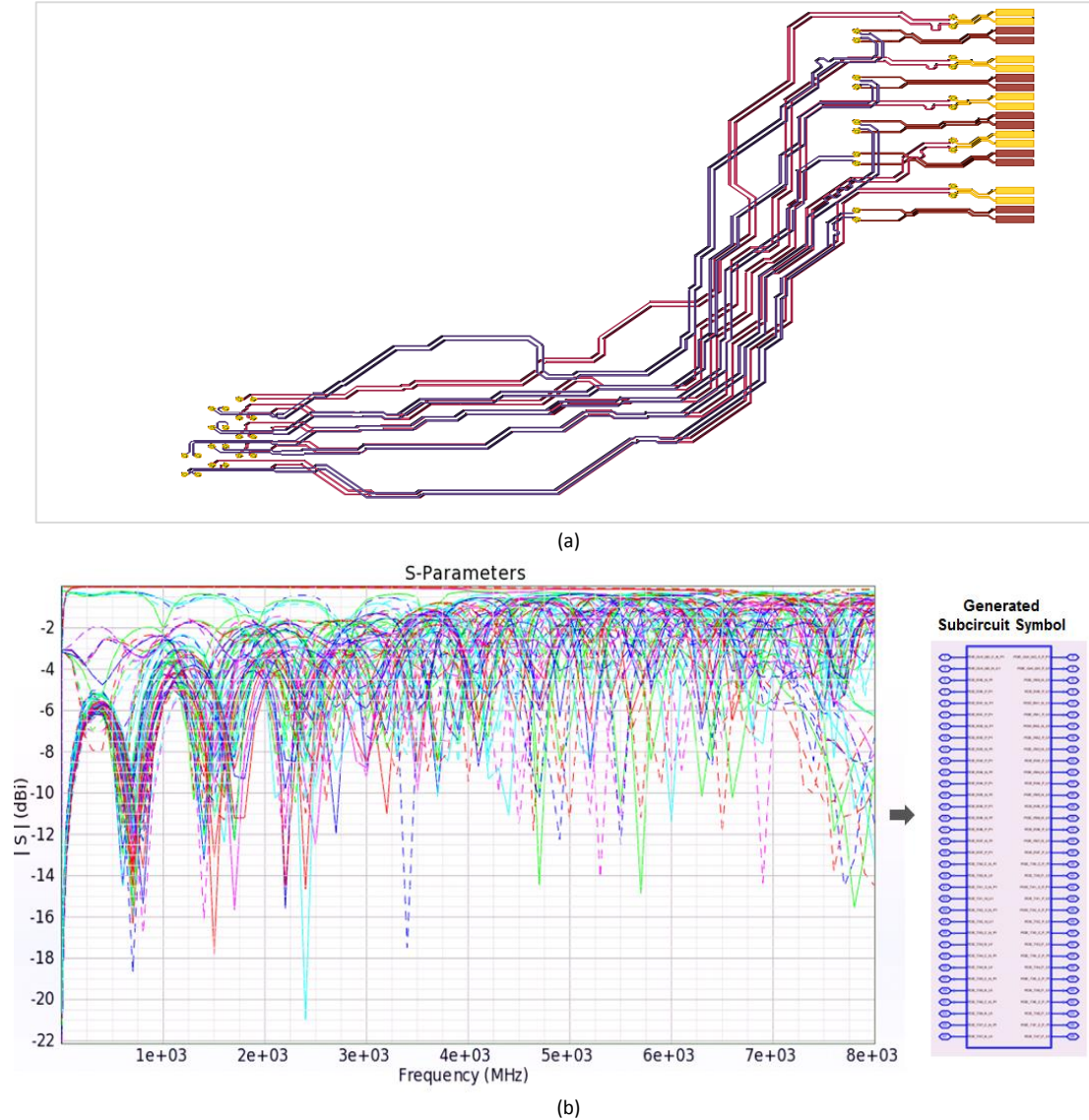


Figure 6: PCIe 3.0 Data Bus in 12-layer FPGA Board (b) Extracted EM data

## 3. Transient Simulation of complete Network

Transient analysis result with PRBS random data input is shown in fig. 7 for complete channel that combines EM extracted data of Connector, eight-lane channel and chip

package. From eye diagram, it can be seen the signal degrades over long transmission path and connectors. The input signal is PRBS-11 serial data at 8-Gb/s.

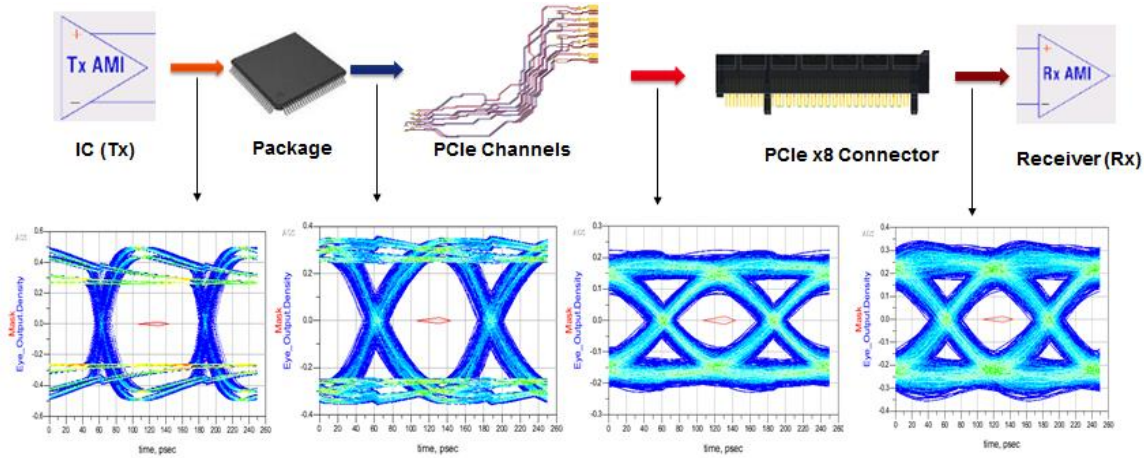


Figure 7: Transient Simulation setup and result for complete Channel

## V.PCie Compliance Testing

Compliance is necessary to ensure products are interoperable. Compliance test is used to validate PCIe channel is compliant with the PCI Express specification. Different compliance test parameters are listed in table II.

Signal	PCie Compliance Testing
Transmitter Electrical	TX Signal Quality Test TX Preset Test
Receiver Electrical	Receiver Jitter Tolerance Test
TX/RX Link equalization	Transmitter initial TX Link EQ Test TX and RX Link Equalization Test
Clock	SSC clock on off testing

TABLE 2 : PCie 3.0 Compliance Testing Parameters

### 1. Transmitter Electrical- TX Signal Integrity

To fully characterize a PCIe transmitter, UI time, Voltages, Eye Mask, Jitter, Idle Timing, Lane Skew are measured based upon the PCI SIG specification. Most specification is required to be measured over 250 consecutive UI (unit intervals). For accurate measurements, a direct connection from the transmitter's TX output to the inputs should be used, this offer the lowest noise measurement. Fig 8 shows eye and jitter measurement on a transmitter transition bit. The eye mask and jitter measurement are made over 250 consecutive UIs. Simulated result is listed in Table III.

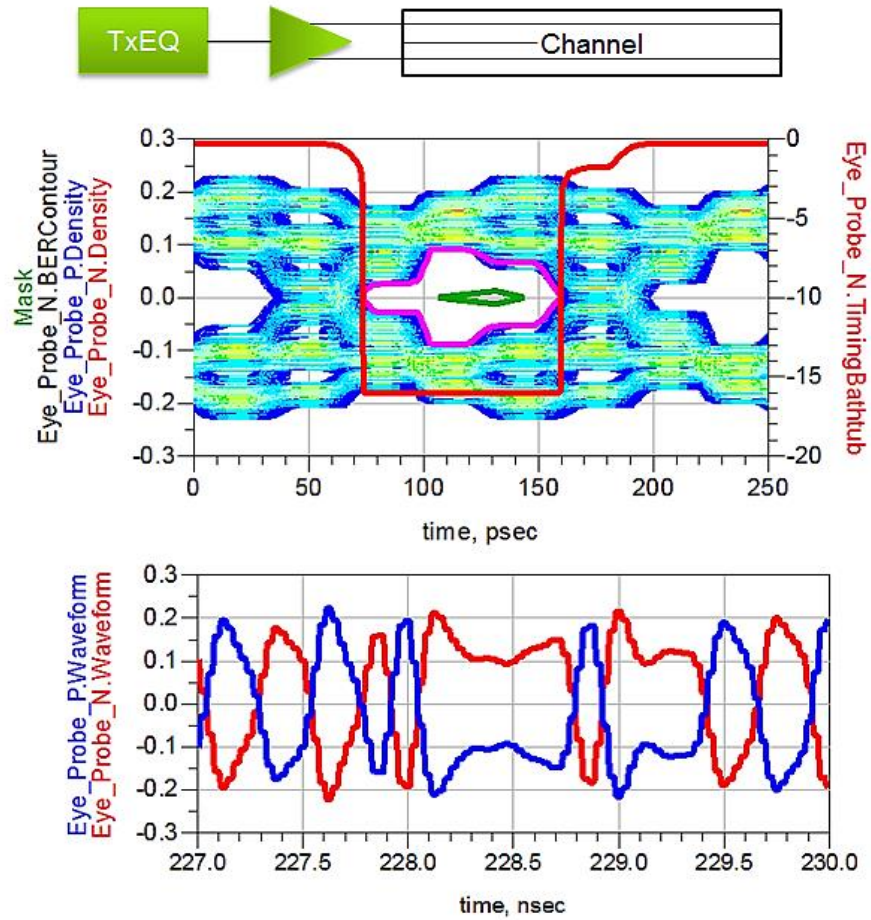


Figure 8: PCIe 3.0 TX Simulation: Eye Diagram and Waveform

Measurement	Result
Eye Height	122.0 mV
Eye Width	86.88 ps
Jitter PP	38.13 ps
Jitter RMS	9.370 ps
Eye Height at BER	180.0 mV
Eye Width at BER	75.83 us

TABLE 3: A Simulation Result of TX

## 2. Receiver Electrical- Equalization

Receivers must be tested for the sensitivity and tolerance to jitter. The testing methodology is to provide a stimulus to the RX input of a device and monitor the response from the device via the TX pins. The measured eye combined with the eye mask

for compliance test. As shown in fig. 9, without any equalization eye is closed and after applying RX equalization eye is open and meeting PCIe specification. The idea behind equalization is to use the voltage levels of the other bits to correct the voltage level of the current bit. Due to the inter-symbol interference (ISI) from the frequency dependent loss of the channel, the eye of the received signals is totally closed, and the clock and data cannot be recovered from the severely distorted signals. After the DFE equalizer, the eye of the equalized signals is opened and the vertical eye opening at the data center is around 368-mV, which is large enough for the decision circuit to recover the digital data at an acceptable BER.

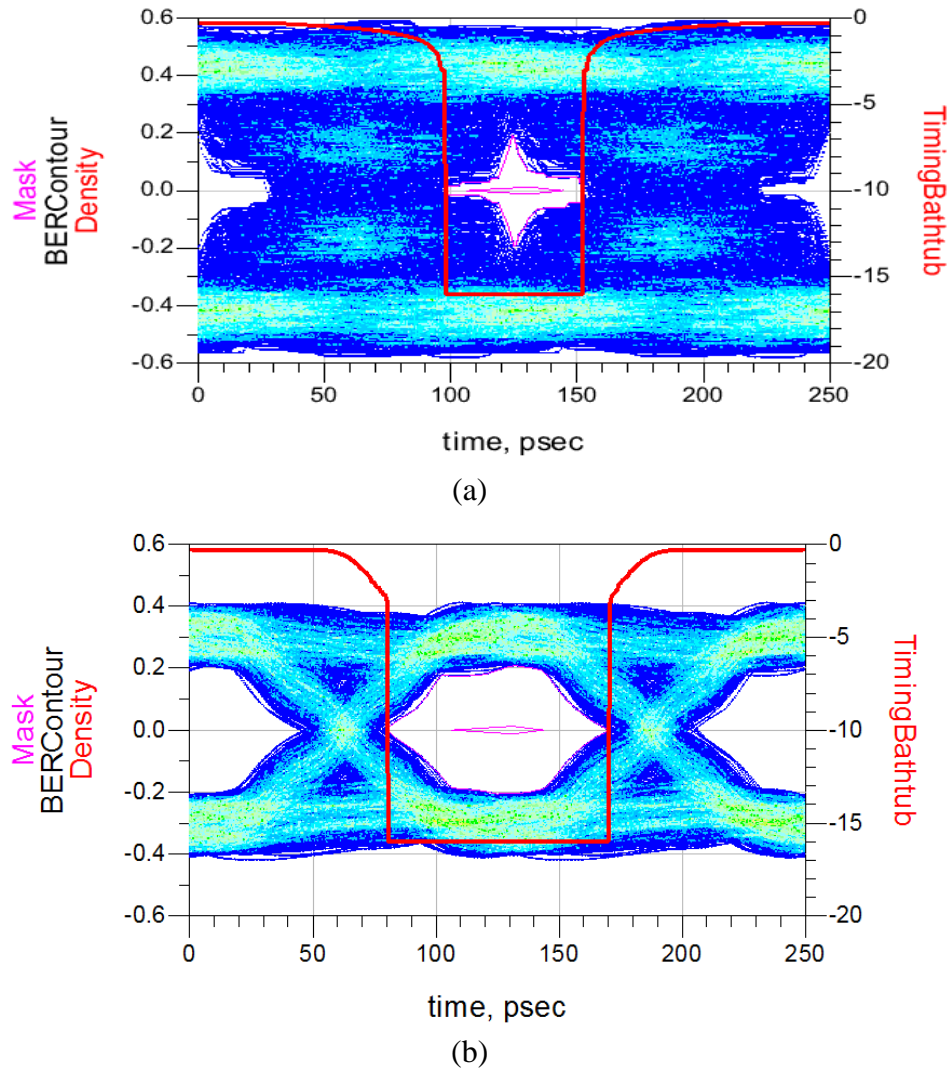


Figure 9: (a) Eye Diagram without Feed-Forward Equalization (FFE) (b) Eye Diagram with Feed-Forward Equalization (FFE)

### 3. TX EQ Setting and Preset Test

PCIe 3.0 specification specifies compliance pattern with 10 presets. Once in compliance mode, bursts of 100MHz clock can be used to cycle through various settings of compliance

patterns to perform, Jitter, voltage, timing measurements. Compliance test ensures DUT can generate all presets and equalization levels meet spec requirements. Fig. 10 shows waveform for all preset values.

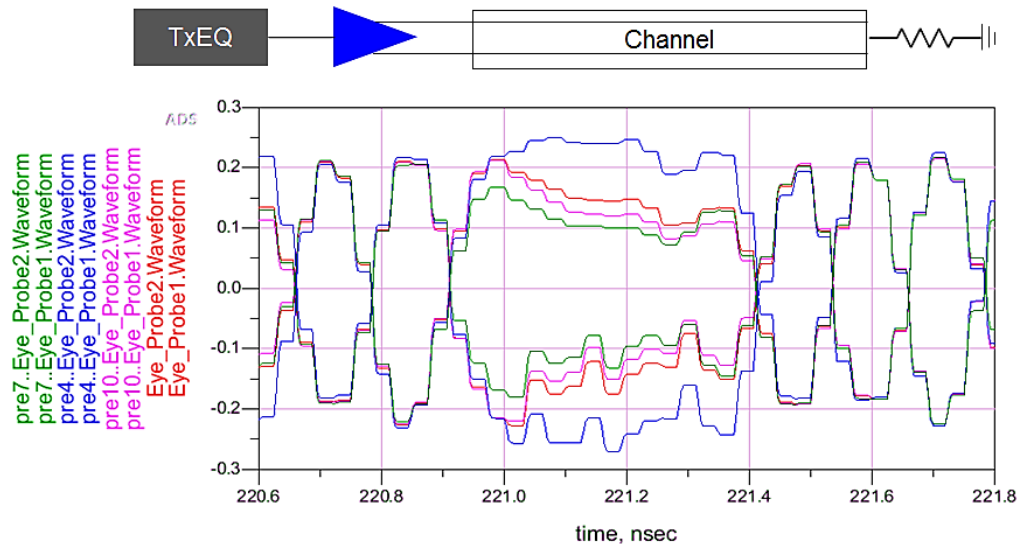


Figure 10: Waveform for different Preset Values

#### 4. Spread Spectrum Clock

The high-speed clocking signals required to drive multiple ICs, however, generate more

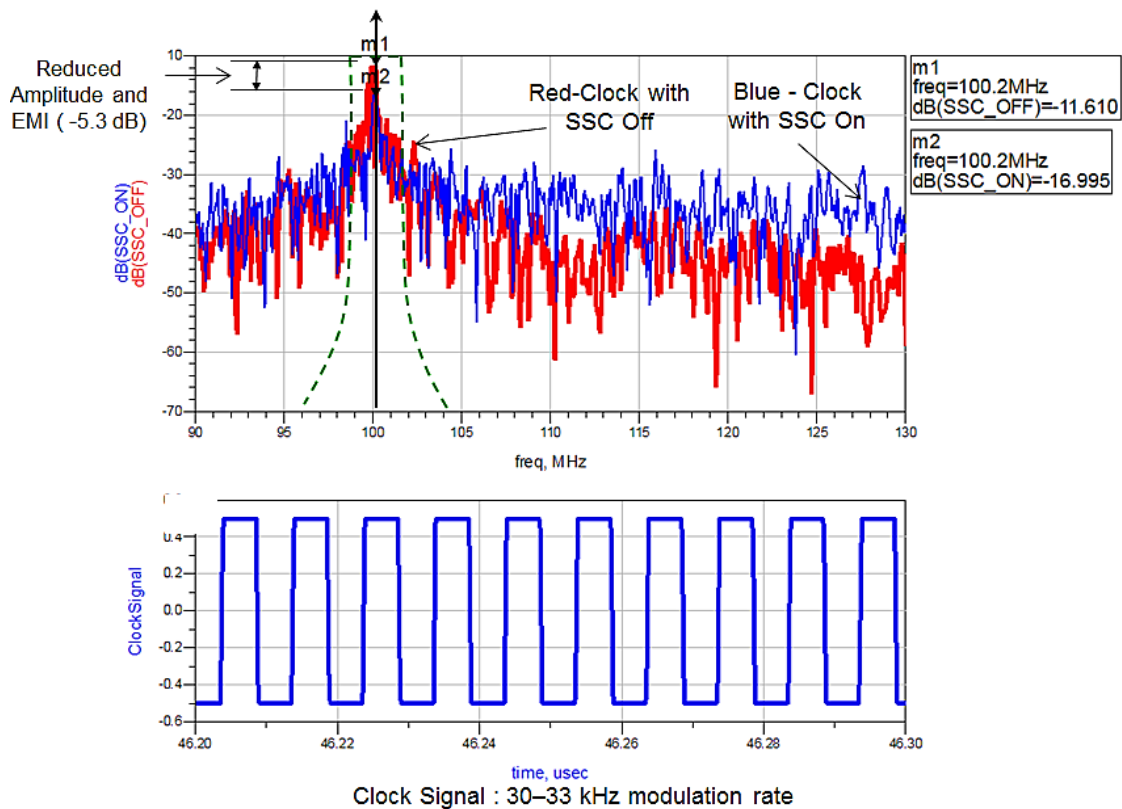


Figure 11: Reducing EMI and Improving Signal Integrity Using Spread Spectrum Clocking

EMI. EMI is one of the major noise sources in high-speed interfaces. If left unattended, these high frequency signals and their harmonics can have peak energy levels that exceed FCC EMI limits.

Several methods for EMI reduction have been used such as shield wires, Vias and coaxial cables. However, spread spectrum clocking (SSC) is most efficient and the simplest method for EMI reduction. Spread Spectrum Clocking is implemented via a 100 MHz reference clock. SSC is a frequency modulation technique, which spreads the clock over larger range. The modulation frequency is usually selected in the range of 30-33 kHz to avoid the cross talk with the audio band. Fig. 11 shows simulation result with and without SSC. After applying SSC EMI level is reduced by -5.3 dB.

## **VI. Conclusion**

In this paper, time domain signal integrity analysis of complete channel of PCIe Gen3 that includes x8 data bus, 3D connector, package, chip package and IBIS-AMI model of TX and RX is presented. Compliance testing of TX and RX electrical as well as complete channel is done to ensure PCIe Gen3 channel performance are meeting PCIe SIG specifications.

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